BLAST specifications	

Unit / Module Name:	BLAST specifications
Unit / Module Number:	N/A
Document Issue:	2.0

Revision History

Date	Revision	Version
03-12-08	Initial release	1.0
06-14-08	Included acronym definition	1.1
08-09-08	Added component envelope	1.2
04-28-10	Made the specifications document generic for use across different form factors	2.0

Related Documents

- IEEE Std 1386.1-2001 : IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC).
- IEEE Std 1386-2001 : IEEE Standard for a Common Mezzanine Card (CMC) Family.

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1 Introduction

BLAST stands for **B**oard **L**evel **A**dvanced **S**calable **T**echnology

The BLAST technology is designed to enhance the FM48x PMC/XMC product series from 4DSP. Connected to a large FPGA, each BLAST can offer in a small form factor a platform for add-on functionality (DRAM memory, SRAM memory, signal processor, microcontroller, video compression/decompression, non volatile flash memory, etc…).

The FM485 and the FM486 are the first product benefiting from this extra flexibility. Up to 4 BLAST are available on the FM485/FM486 (FPGA A BLAST is restricted to 72 pins).

Each BLAST offers up to 100 I/O and is available as a 160-pin Ball Grid Array (BGA) component that can be mounted on the PMC/XMC on request.

2 Dimensions

The BLAST technology is available in two dimensions that have been carefully considered so it can fit on convection and conduction cooled PMC/XMC products.

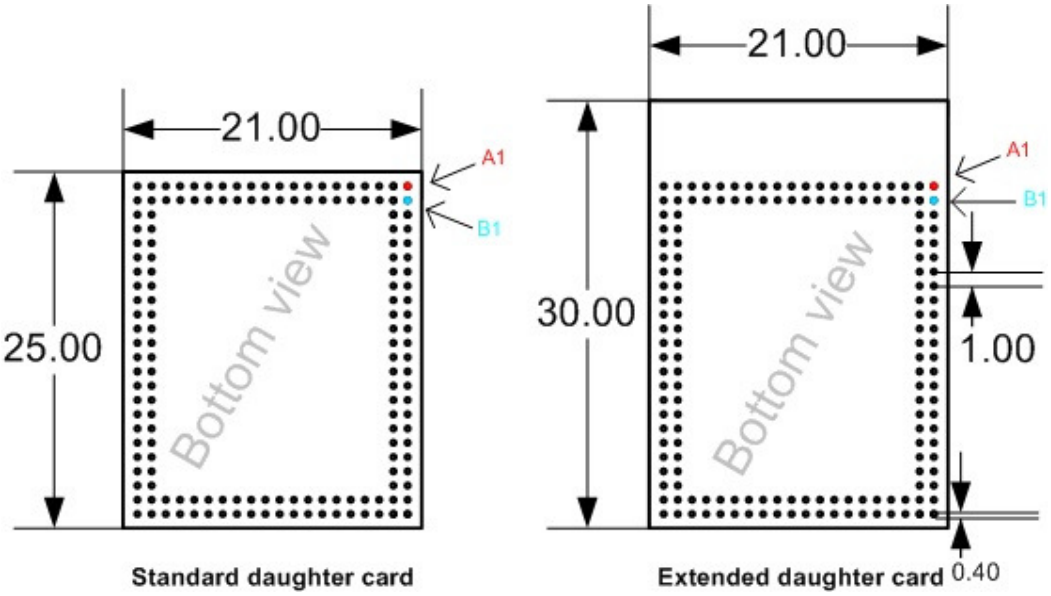


Figure 1 : BLAST and eBLAST dimensions

For compliance to the IEEE Std 1386.1-2001, restrictions in height for BLAST are a primary concern. The height should not exceed 4.7mm from the base of the PMC/XMC. The added height of the BLAST PCB and the collapsed BGA balls should be 2mm (1.6mm PCB thickness). This leaves 2.7mm available for the component envelope. Most devices considered for BLAST applications will fit in this envelope.

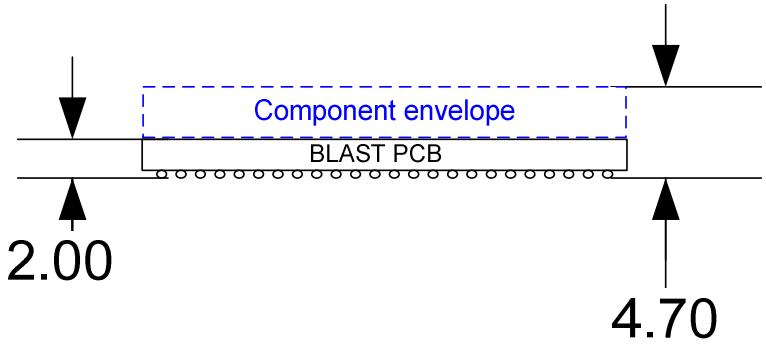


Figure 2 : BLAST height and component envelope

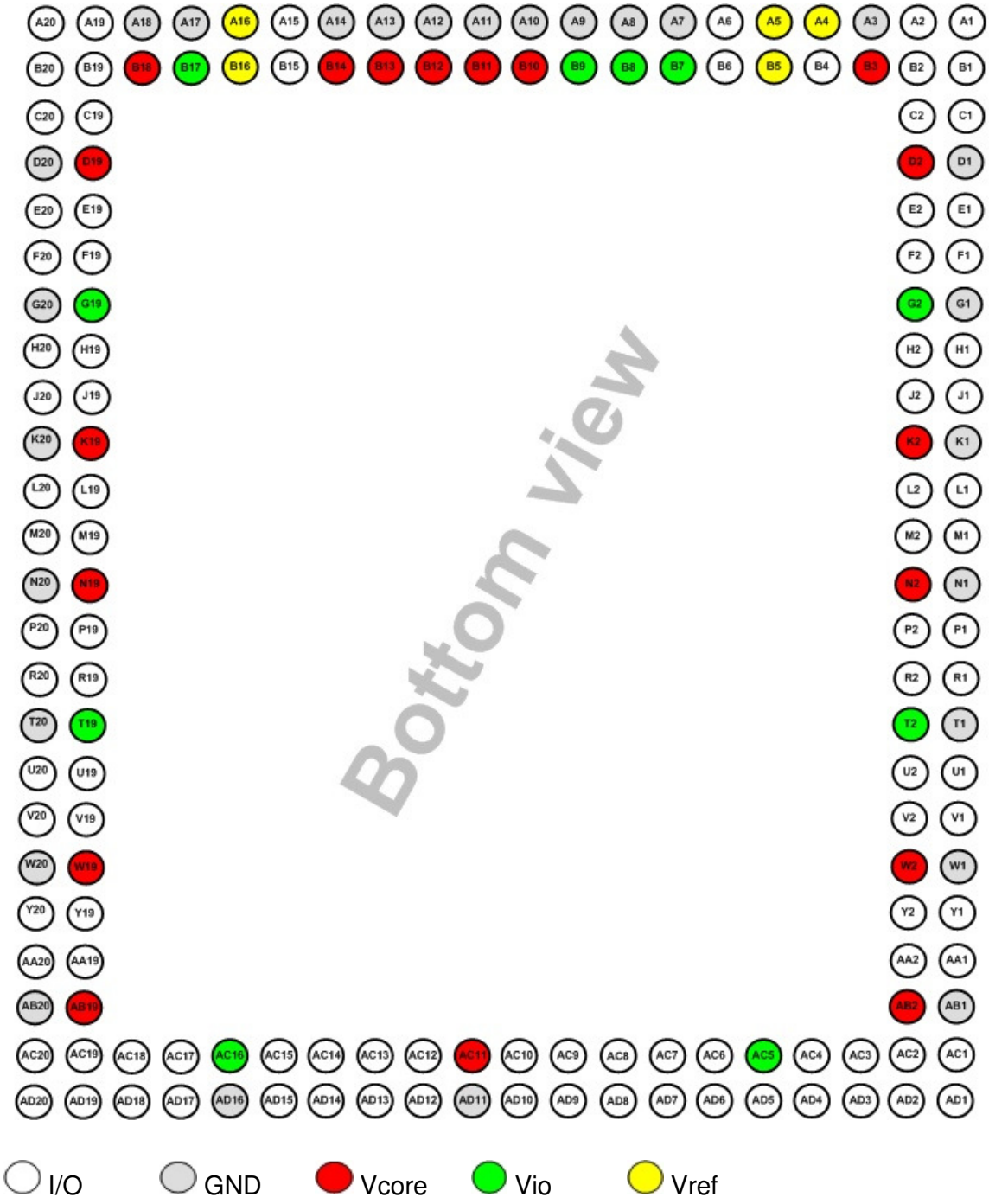


Figure 3 : BLAST pin numbering

Please note that pins A5 to A16 and B5 to B16 are optionally No Connect. This facilitates the placement of components in the extra area offered by the extended version of BLAST. Designers must however be aware that even if these balls are optionally No Connect, it is important that they are available mechanically to ensure a proper and balanced assembly process when a BLAST is placed onto the PMC/XMC.

3 BLAST Pinout

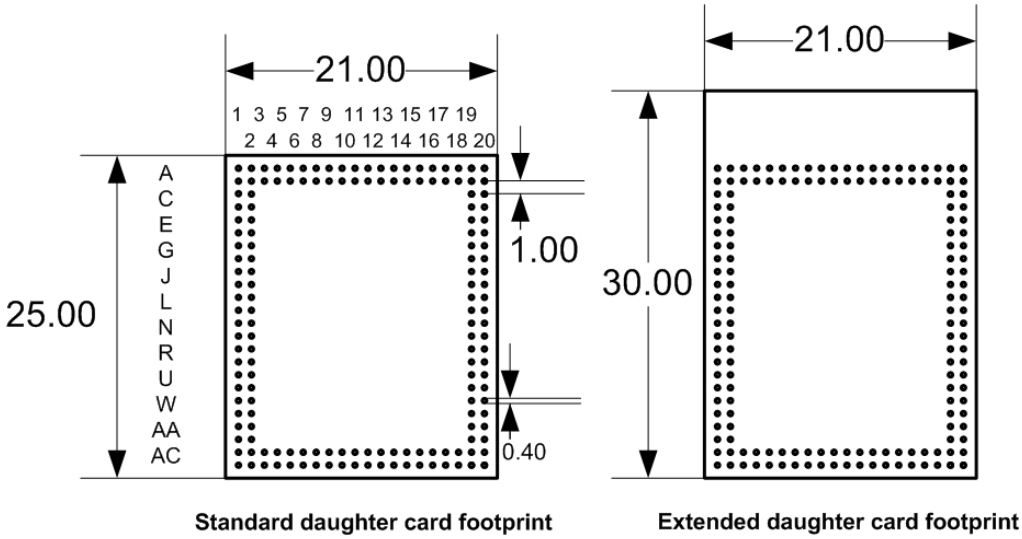
Ball number	Function	Description
A1, A2, A6, A15, A19, A20 B1, B2, B4, B6, B15, B19, B20 C1, C2, C19, C20 E1, E2, E19, E20, F1, F2, F19, F20, H1, H2, H19, H20, J1, J2, J19, J20, L1, L2, L19, L20, M1, M2, M19, M20, R1, R2, R19, R20, U1, U2, U19, U20, V1, V2, V19, V20, Y1, Y2, Y19, Y20, AA1, AA2, AA19, AA20, AC1 to AC4, AC6 to AC10, AC12 to AC15, AC17 to AC20, AD1 to AD10, AD12 to AD15, AD17 to AD20	I/O	Input/Output signals Pairs (1-2, 19-20) are connected to adjacent signals on the FPGA base board. These pairs should be used on BLAST in the case a differential clock signals is routed from the FPGA to BLAST.
P1, P2, P19, P20	Clocks	Clock capable I/Os on the FPGA base board. Can be used as standard I/O.
A3, A7 to A14, A17, A18, D1, D20, G1, G20, K1, K20, N1, N20, T1, T20, W1, W20, AB1, AB20, AD11, AD16	GND	Ground signal
B3, B10 to B14, B18, D2, D19, K2, K19, N2, N19, W2, W19 AB2, AB19, AC11	Vcore	Voltage for device core. Typically 1.2V, 1.5V or 1.8V
B4, B7 to B9, B17, G2, G19, T2, T19, AC5, AC16	VIO	Voltage for device I/Os Typically 1.5V, 1.8V or 3.3V
A4, A5, A16, B5, B16	Vref	Voltage reference for memory applications. Typically 0.75V or 0.9V

Table 1: BLAST pinout

Please note that ball numbers in blue in the table above are optionally No Connect.

4 Base card footprint

A BLAST will typically be assembled on PMC/XMC base card. The recommended footprint is shown below.



Standard daughter card footprint **Extended daughter card footprint**

Figure 4 : Base card recommended footprint (top view)